Micro Power Systems

MP7685

CMOS
11-Bit, Low Power
Analog-to-Digital Converter

FEATURES

- Sampling Rate from 1 kHz to 1 MHz
- Very Low Power CMOS - 100 mW (max)
- Interface to any Input Range between GND and V_{DD}
- No Sample/Hold needed for Input Signals Less Than 10 KHz
- Single Power Supply (4 to 6.5 Volts)
- TTL Compatible Tri-State Outputs
- Latch-Up Free CMOS Technology
- 2000 V ESD Protection
- CDIP & PDIP Packages Available
- Not Recommended for New Design – See MP7695

BENEFITS

- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- Low Power A/D Applications
- High Resolution Imaging
- Multiplexed Data Acquisition
- Radar Pulse Analysis

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GENERAL DESCRIPTION

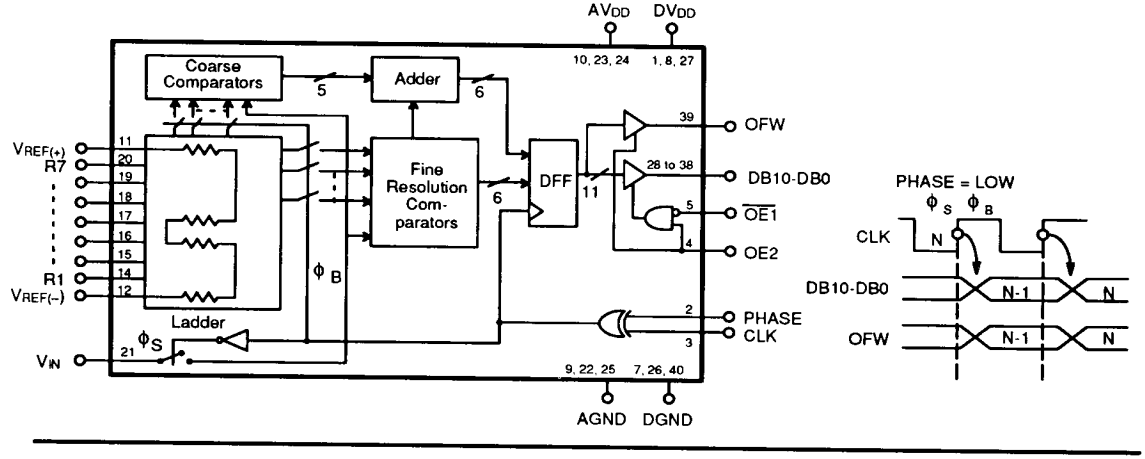
The MP7685 is a 11-bit monolithic CMOS analog-to-digital converter designed for precision applications demanding *Low Power Consumption*. The input architecture of the MP7685 allows direct interface to any analog input range between GND and V_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The Micro Power Systems' MP7685 uses a two-step flash technique. The first segment converts the 5 MSBs and consists of 31 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

With 100 mW power dissipation, the MP7685 achieves its excellent performance due to the inherent high speed of our proprietary 2 Micron CMOS Process.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7685 is available in Plastic and Ceramic dual-in-line packages.

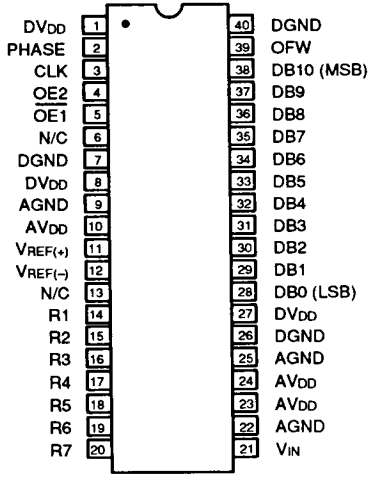
SIMPLIFIED BLOCK AND TIMING DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (± LSBs)	INL (± LSBs)
Plastic Dip	–40 to +85°C	MP7685JN	2 1/4	2 1/4
Ceramic Dip	–40 to +85°C	MP7685JD	2 1/4	2 1/4
Ceramic Dip	–40 to +85°C	MP7685KD	2 1/4	2 1/4
Ceramic Dip	–55 to +125°C	MP7685SD	2 1/4	2 1/4
Ceramic Dip	–55 to +125°C	MP7685SD/883	2 1/4	2 1/4
Ceramic Dip	–55 to +125°C	MP7685TD	2 1/4	2 1/4
Ceramic Dip	–55 to +125°C	MP7685TD/883	2 1/4	2 1/4

PIN CONFIGURATION



40 Pin CDIP, PDIP (0.600")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DV_{DD}	Digital Power Supply
2	PHASE	Sampling Phase Control
3	CLK	Clock Input
4	$\overline{OE2}$	Chip Output Enable
5	$\overline{OE1}$	Chip Output Enable
6	N/C	No Connection
7	DGND	Digital Ground
8	DV_{DD}	Digital Power Supply
9	AGND	Analog Ground
10	AV_{DD}	Analog Power Supply
11	$V_{REF(+)}$	Reference Voltage (+) Supply
12	$V_{REF(-)}$	Reference Voltage (–) Supply
13	N/C	No Connection
14	R1	Ladder Tap 1
15	R2	Ladder Tap 2
16	R3	Ladder Tap 3
17	R4	Ladder Tap 4
18	R5	Ladder Tap 5
19	R6	Ladder Tap 6
20	R7	Ladder Tap 7
21	V_{IN}	Analog Input
22	AGND	Analog Ground
23	AV_{DD}	Analog Power Supply
24	AV_{DD}	Analog Power Supply
25	AGND	Analog Ground
26	DGND	Digital Ground
27	DV_{DD}	Digital Power Supply
28	DB0	Output Data Bit 0 (LSB)
29	DB1	Output Data Bit 1
30	DB2	Output Data Bit 2
31	DB3	Output Data Bit 3
32	DB4	Output Data Bit 4
33	DB5	Output Data Bit 5
34	DB6	Output Data Bit 6
35	DB7	Output Data Bit 7
36	DB8	Output Data Bit 8
37	DB9	Output Data Bit 9
38	DB10	Output Data Bit 10 (MSB)
39	OFW	Output Overflow Bit
40	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 1.0 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		11			11		Bits	
Sampling Rate	F_S	0.001		1	0.001	1	MHz	
ACCURACY (J, S Grades) (1)								
Differential Non-Linearity	DNL			±2		±2 1/4	LSB	F_S = 0.5 MHz
Integral Non-Linearity	INL			±2		±2 1/4	LSB	Best Fit Line (Max INL – Min INL) / 2
ACCURACY (K, T Grades) (1)								
Differential Non-Linearity	DNL			±2		±2 1/4	LSB	F_S = 1 MHz
Integral Non-Linearity	INL			±2		±2 1/4	LSB	Best Fit Line (Max INL – Min INL) / 2
REFERENCE VOLTAGES								
Positive Ref. Voltage (2)	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Ladder Resistance	R_L	1		3	0.7	3.9	KΩ	
Ladder Temp. Coefficient (3)	R_{TCO}					3000	ppm/°C	
ANALOG INPUT (3)								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance (4)	C_{INA}		60				pF	
Aperture Delay (5)	t_{AP}		50				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		31				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents (6)								V_{IN}=GND to V_{DD}
CLK	I_{IN}			±100	−150	150	µA	
PHASE		−1		75	−1	100	µA	
OE2		−75		1	−100	1	µA	
$\overline{OE1}$		−1		75	−1	100	µA	
Input Capacitance (3)	C_{IND}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	1			1		µs	
Duty Cycle			50				%	
Rise Time (5)	t_R			10			ns	
Fall Time (5)	t_F			10			ns	

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ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.6					V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.3			V	I_{LOAD} = 1.0 mA
Tristate Leakage	I_{OZ}			±1		±11	µA	V_{OUT}=GND to V_{DD}
Data Hold Time (*See Figure 1.*) (3)	t_{HLD}		50				ns	
Data Valid Delay (3)	t_{DL}		66				ns	
Data Enable Delay (3)	t_{DEN}		40				ns	
Data Tristate Delay (3)	t_{DHZ}		40				ns	
POWER SUPPLIES (7, 8)								
Operating Voltage (AV_{DD}, DV_{DD})	(3) V_{DD}	4	5	6			V	
Current (AV_{DD} + DV_{DD})	I_{DD}			20		30	mA	

NOTES

(1) Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/2048) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (Fs).

(2) For best results it is recommended that the reference voltage be limited to (V_{DD} – .5 V) maximum.

(3) Guaranteed. Not tested.

(4) See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

(5) Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

(6) All digital inputs have protection diodes to V_{DD} and GND. Phase and $\overline{OE1}$ have internal pull down resistors; OE2 has internal pull up resistors. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

(7) DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

(8) AV_{DD} should be tied to DV_{DD} at the package, DGND should be tied to AGND at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{DD} (to GND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP 1500mW

Derates above 75°C ..... 20mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

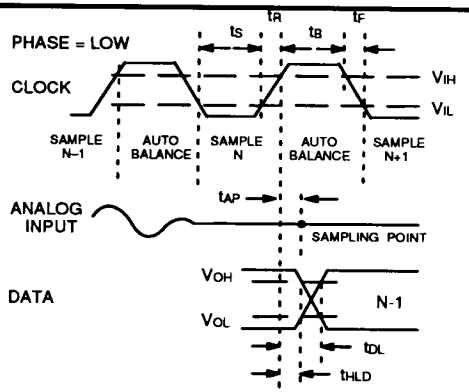

Figure 1. MP7685 Timing Diagram

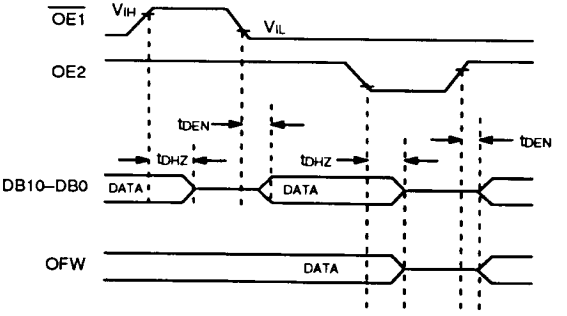

Figure 2. Output Enable/Disable Timing Diagram

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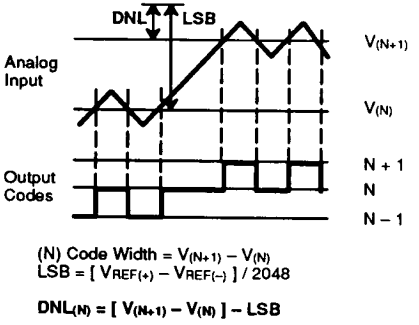

Figure 3. DNL Measurement On Production Tester

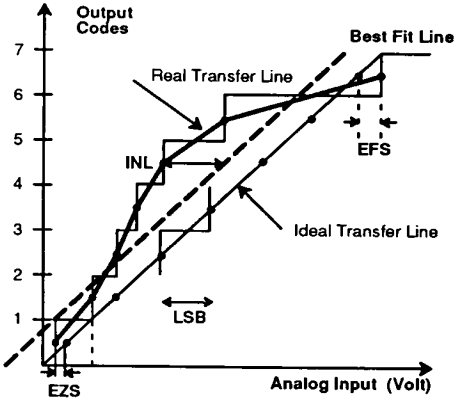

Figure 4. INL Error Calculation (Exaggerated for Visualization)

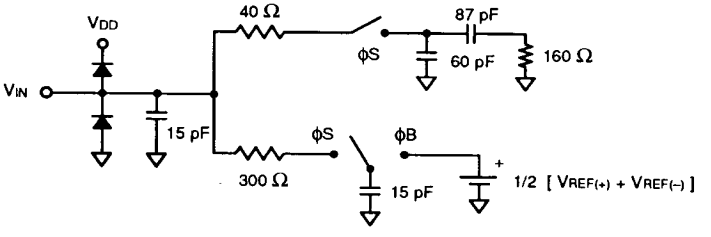

Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7685 converts analog voltages into 2048 digital codes by encoding the outputs of 31 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 2049 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relationships apply:

$R_{REF} = 2048 * R \qquad V_{REF} = V_{REF(+)} - V_{REF(-)} = 2048 * LSB$

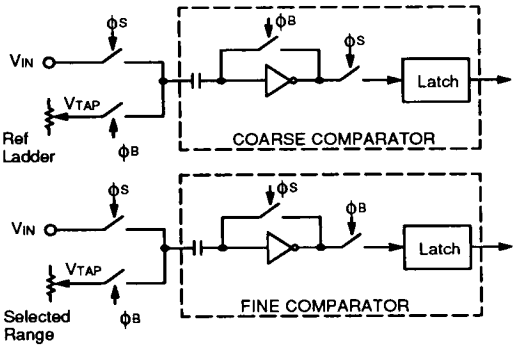

Figure 6. MP7685 Comparators

The clock signal generates the two internal phases, ϕ_B and ϕ_S (*See Figure 6.*). When the phase pin is low, the rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects V_{IN} from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

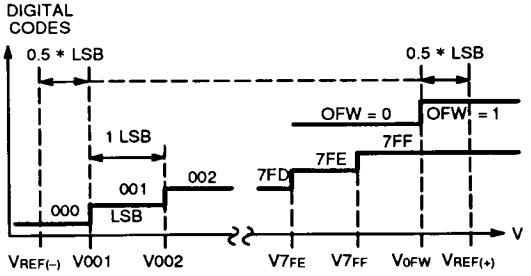

Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V7_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 2048 = (V7_{FF} - V001) / 2046$

Note that the overflow transition is a flag and has no impact on the data bits.

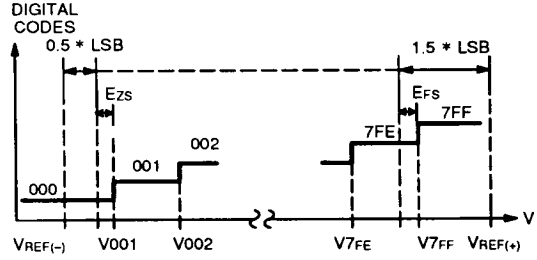

Figure 8. Real A/D Transfer Curve

In a "real" converter the code-to-code transitions do not fall exactly every $V_{REF}/2048$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 2.25 mV and every code width is within 1.125 and 3.375 mV of the ideal code width.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

$DNL\ (001) = V002 - V001 - LSB$

: : :

$DNL\ (7FE) = V7_{FF} - V7_{FE} - LSB$

E_{ZS} (zero scale error) $= V7_{FF} - V_{REF(+)} + (1.5 * LSB) - V7_{FF}$

E_{ZS} (zero scale error) $= V001 - V_{REF(-)} - (1.5 * LSB)$

Figure 8. shows the zero scale and full scale error terms.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and and the negative INL errors. INL max errors at –1 and +2 LSBs would have a best fit line INL errors of (+2 – (–1)) / 2 = 1.5 LSB.

Clock and Conversion Timing

A system will clock the MP7685 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9a* shows normal operation, while the timing of *Figure 9b* keeps the MP7685 in balance and ready to sample the analog input.

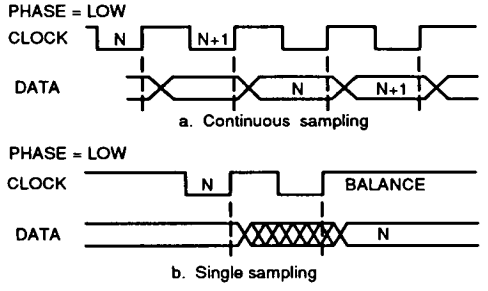

Figure 9. Relationship of Data to Clock

Analog Input

The MP7685 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. However, a more common use of this flexibility is to first design the analog circuitry and then adjust the reference voltages to include the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds. It is good design practice to proceed with these steps:

1) Estimate V_{REF} range.
2) Design analog circuitry.
3) Prototype analog circuitry and debug with ADC clocked.
4) Adjust V_{REF} range.

To guarantee optimization of the MP7685, the circuit driving the flash analog input must have good output drive capabilities (low resistance, high current).

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 2048 * (A_{IN}/V_{REF})$$
for $V_{IN} > (V_{REF(+)} - 1\ LSB)$, DATA = 7FF

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB10 - DB0
1	1	Valid	High Z
0	1	Valid	Valid
X	0	High Z	High Z

Table 1. Output Enable Logic

The functional equivalent of the MP7685 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕs).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts VIN with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

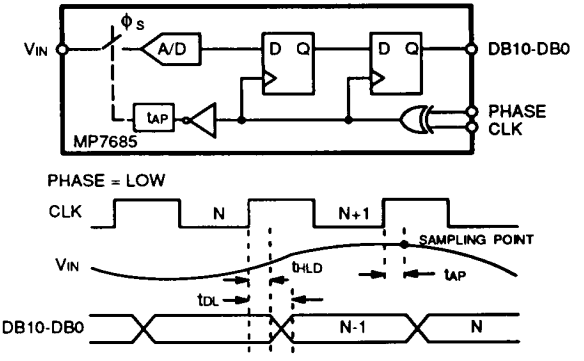

Figure 10. MP7685 Functional Equivalent Circuit and Interface Timing

HARMONIC DISTORTION