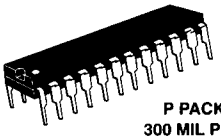
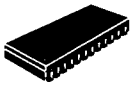
MCM6290C

16K x 4 Bit Static RAM
With Output Enable



P PACKAGE
300 MIL PLASTIC
CASE 724A



J PACKAGE
300 MIL SOJ
CASE 810A

3

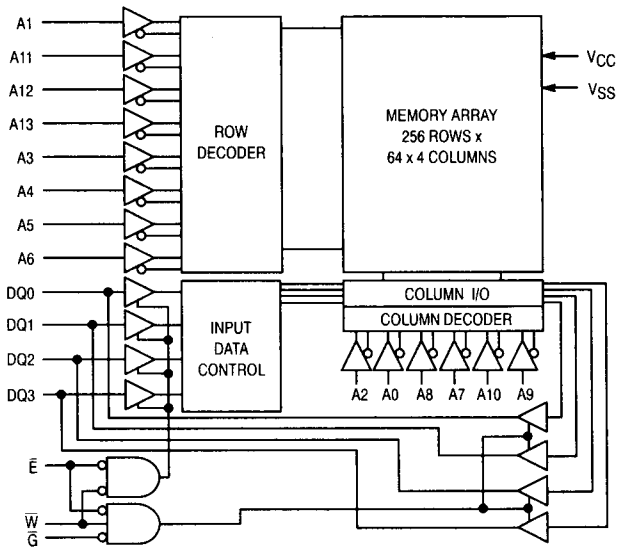
The MCM6290C (with output enable) is a 65,536 bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access time performance.

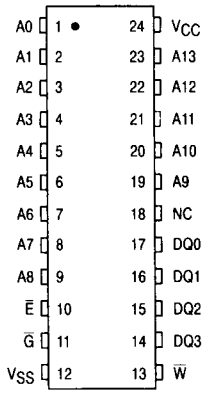
The MCM6290C has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V ± 10% Power Supply
- Low Power Operation: 120 mA Maximum, Active AC
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 10, 12, 15, 20, 25, 35 ns
- Two Chip Controls:
  - $\overline{E}$ for Automatic Power Down
  - $\overline{G}$ for Fast Access to Data and Elimination of Bus Contention Problems
- Fully TTL Compatible — Three-State Data Output

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A13	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z
L	H	H	Output Disabled	I_{CCA}	High-Z
L	L	H	Read	I_{CCA}	D_{out}
L	X	L	Write	I_{CCA}	D_{in}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 10	- 12	- 15	- 20	- 25	- 35	Unit
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	120	120	120	110	110	110	mA
Standby Current (TTL Levels, V_{CC} = Max)	I_{SB1}	50	45	40	35	30	30	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Address and Control Input Capacitance	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameters	Symbol		-10		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	5	—	6	—	8	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	5	0	6	0	8	0	8	0	10	0	15	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	5	0	6	0	7	0	8	0	10	0	15	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	10	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. .For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

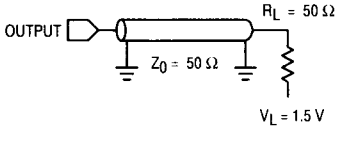


Figure 1A

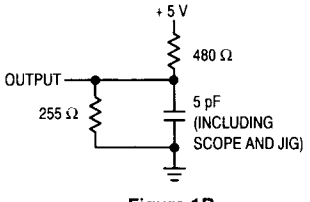


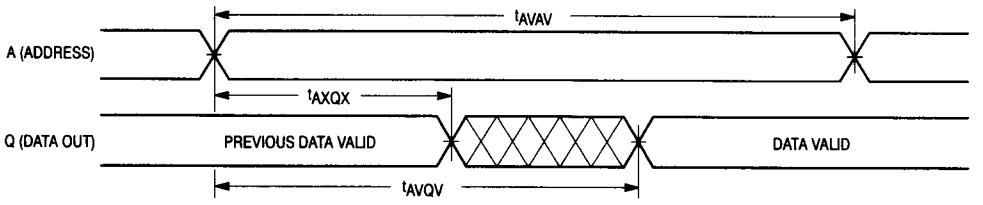
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



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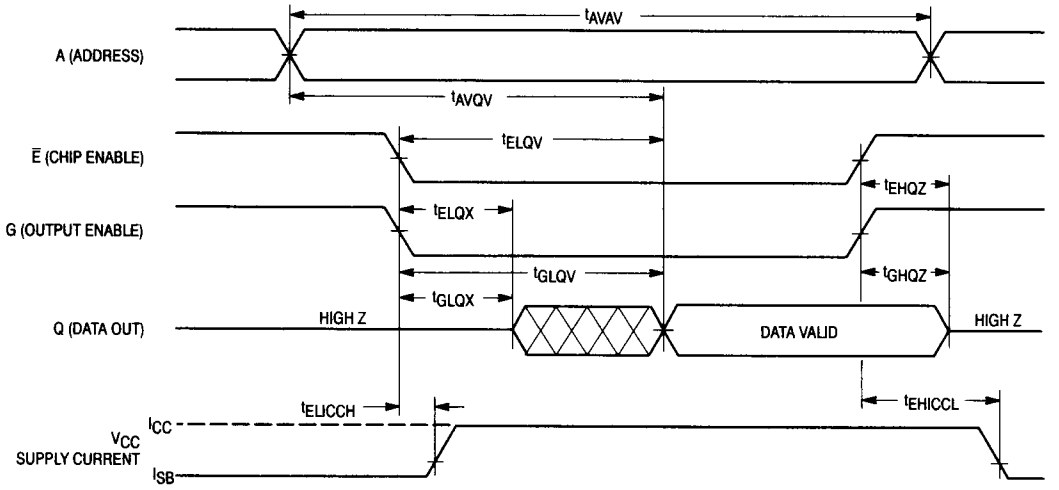
READ CYCLE 2 (See Notes 2 and 4)

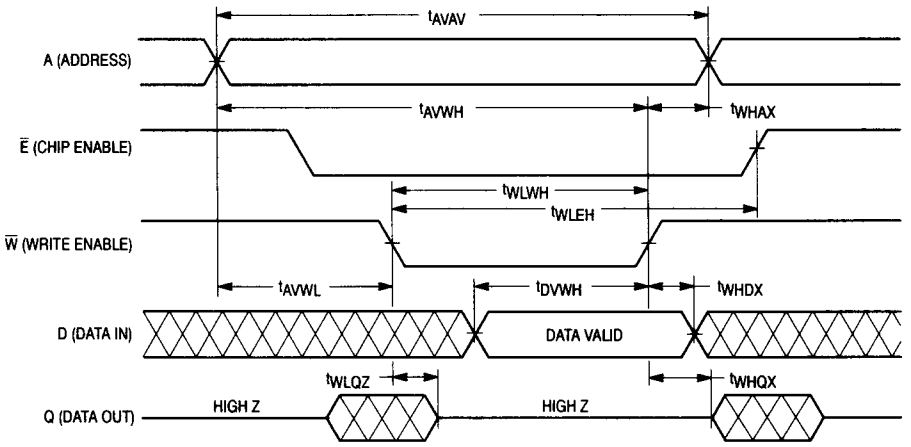


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		- 10		- 12		- 15		- 20		- 25		- 35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	9	—	10	—	12	—	15	—	20	—	30	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	7	—	8	—	10	—	12	—	15	—	25	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	7	0	8	0	10	0	15	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

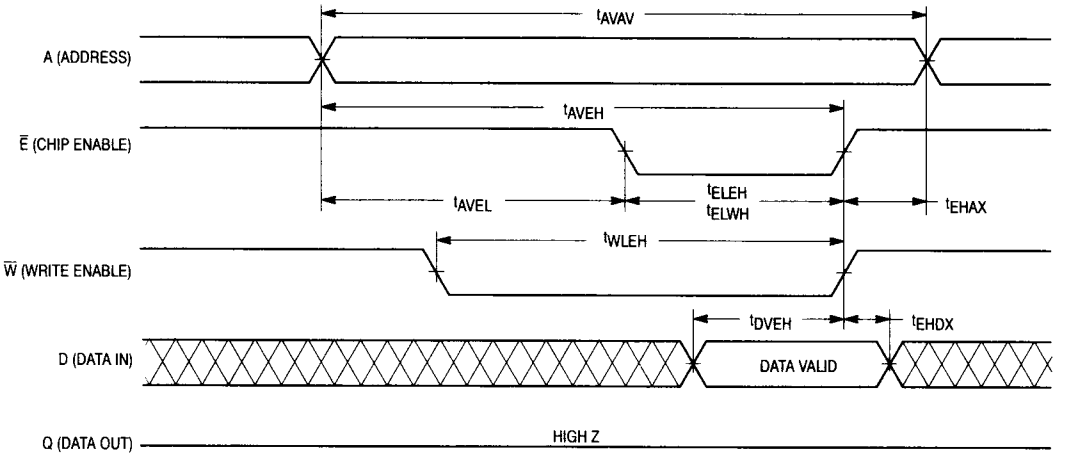


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		- 10		- 12		- 15		- 20		- 25		- 35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	8	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	7	—	8	—	10	—	12	—	15	—	25	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6290C X XX XX

- MCM — Motorola Memory Prefix
- 6290C — Part Number
- XX — Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)
- X — Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers —

MCM6290CP12	MCM6290CJ10	MCM6290CJ10R2
MCM6290CP15	MCM6290CJ12	MCM6290CJ12R2
MCM6290CP20	MCM6290CJ15	MCM6290CJ15R2
MCM6290CP25	MCM6290CJ20	MCM6290CJ20R2
MCM6290CP35	MCM6290CJ25	MCM6290CJ25R2
	MCM6290CJ35	MCM6290CJ35R2